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I refer to TM4C1231H6PGE and its datasheet. The description of SSI Interrupt Mask (SSIIM) (pag. 954) is a little bit confusing. 0 The transmit FIFO interrupt is masked. (I understand that the ...

SSI interrupt mask

However, in the datasheet (DS-TM4C1231H6PM-15553.2700), the bit 0x20 is specified as reserved in Register 6: SSI Interrupt Mask (SSIIM), offset 0x014. I need to know the exact behaviour of this ...

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